WHAT IS CLAIMED IS:

1. A semiconductor device having, when one of either an N-type or P-type is defined as a first conductivity type, and the other is defined as a second conductivity type,

a semiconductor substrate of the first conductivity type, the semiconductor device comprising:

first and second buried layers provided within the semiconductor substrate, being of the first conductivity type, and being of a higher concentration than the semiconductor substrate;

first and second emitter layers of the first conductivity type;

first and second base layers of the second conductivity type;

and a substrate layer constituted by the semiconductor substrate,

wherein the substrate layer is sandwiched between the first and second buried layers,

wherein the first and second base layers are positioned on one side surface and the other side surface of the semiconductor substrate so as to form PN junctions with the first and second buried layers,

wherein the first and second emitter layers are located in a vicinity of a surface of inside of the first and second base layers so as to form PN junctions with the first and second

base layers,

wherein at least a part of the first and second base layers are respectively provided between the first and second emitter layers and the first and second buried layers, and

wherein at least a part of the first and second buried layers are located between the first and second base layers the substrate layer.

2. The semiconductor device of claim 1, wherein first and second metal films are formed on both sides of the semiconductor substrate, the first emitter layer and the first base layer being electrically short-circuited by the first metal film, and the second emitter layer and the second base layer being electrically short-circuited by the second metal film.

3. The semiconductor device of claim 2, wherein ring-shaped first and second moats with bottom surfaces reaching the buried layers are formed on both sides of the semiconductor substrate, and wherein the first and second emitter layers are located on inside of the first and second moats.

4. The semiconductor device of claim 3, wherein the insides of the first and second moats are filled with oxide.

5. The semiconductor device of claim 3, wherein at least a part

of the first and second base layers are positioned at a region on outside of the first and second moats of the surfaces of the semiconductor substrate.

6. The semiconductor device of claim 3, wherein at least a part of the first and second buried layers are positioned at a region on the outside of the first and second moats of the surfaces of the semiconductor substrate.

7. A semiconductor device manufacturing method comprising, when one of an N-type and P-type is defined as a first conductivity type and the other is defined as a second conductivity type, the steps of:

forming a first buried layer of the first conductivity type in a vicinity of a surface at inside of one side of a semiconductor substrate of the first conductivity type and forming a second buried layer of the first conductivity type in a vicinity of a surface of the other side, in such a manner that the first and second buried layers sandwich a substrate layer composed of a remaining portion of the semiconductor substrate;

forming first and second base layers of the second conductivity type in a vicinity of surfaces at insides of the first and second buried layers in such a manner that bottom surfaces are positioned in the first and second buried layers;

and

forming first and second emitter layers of the first conductivity type in vicinity of surfaces at insides of the first and second base layers so that bottom surfaces thereof are positioned in the first and second base layers.

8. The semiconductor device manufacturing method of claim 7, wherein the first and second buried layers are formed by introducing an impurity of the first conductivity type into the semiconductor substrate with surfaces of both sides of the semiconductor substrate completely exposed and diffusing impurity of the first conductivity type.

9. The semiconductor device manufacturing method of claim 8, wherein the first and second base layers are formed by introducing an impurity of the second conductivity type into the first and second buried layers with the surfaces of the first and second buried layers completely exposed and diffusing impurity of the second conductivity type.

10. The semiconductor device manufacturing method of claim 7, further comprising, with ring-shaped moats having bottom surfaces reaching positions deeper than bottom surfaces of the base layers, a step of forming moats including the first and second emitter layers inside of the ring-shaped moats on both

sides of the semiconductor substrate.

11. The semiconductor device manufacturing method of claim 10, further comprising a step of forming first and second metal films short-circuiting the first and second emitter layers positioned inside of the ring-shaped moats and the first and second base layers after filling insides of the first and second moats with oxide and forming first and second passivation films.